IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michele J. Berry	Examiner: Luan C. Thai
Serial No.:	09/965,555	Group Art Unit: 2827
Filed:	September 27, 2001	Docket: 884.548US1
Title:	ENCAPSULATION OF PIN SOLDER FOR MAINTAINING ACCURACY IN PIN POSITION	

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a two-month extension of the period for responding to the Office action, thereby moving the deadline for response from 18 October 2002 to 18 December 2002.

In response to the Office Action dated 18 July 2002, please amend the above-identified patent application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect an amendment of claims 10 and 11 and an addition of new claims 23-35. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the following claims:

10. (Amended) A method for use during fabrication of a microelectronic device package, comprising:

providing a package substrate having a plurality of contact pads on a surface thereof;

attaching individual pins to said plurality of contact pads by solder reflow; and

selectively applying an encapsulation material about solder joints associated with said individual pins, said encapsulation material to maintain a location of said individual pins on said package substrate during subsequent high temperature processing.

11. (Amended) The method of claim 10, wherein attaching individual pins includes:

placing said individual pins in a jig;

applying solder to at least one of the following: said individual pins and said contact pads;

aligning said jig with said package substrate; and

applying pressure to said jig at a temperature that equals or exceeds a melting temperature of said solder.

Please add the following new claims:

23. (New) A method for use in assembling a microelectronic circuit package, comprising:

applying a polymer material to a surface of a package substrate;

attaching pins to said package substrate, through said polymer material, by solder reflow; and

allowing said polymer material to cure about solder joints associated with said pins.

24. (New) The method of claim 23, wherein:

attaching pins includes placing solder elements in the polymer material in desired pin locations.

25. (New) The method of claim 24, wherein:

said solder elements include solder balls.

26. (New) The method of claim 24, wherein:

attaching pins includes pressing a pin toward said package substrate at the location of a solder element.

27. (New) The method of claim 24, wherein:

attaching pins includes using a jig to press multiple pins toward said package substrate at the locations of solder elements.

28. (New) The method of claim 23, wherein:

applying a polymer material includes screen printing said material on said surface.

29. (New) The method of claim 23, wherein:

attaching pins to said package substrate includes placing said pins in a jig and applying pressure to said jig at a temperature that equals or exceeds a melting temperature of the pin solder so that the pins are pressed through the polymer material.

30. (New) The method of claim 23, wherein:

said polymer material includes a no flow material.

31. (New) The method of claim 23, wherein:

said polymer material has fluxing capabilities.

32. (New) A method for use during fabrication of a microelectronic device package, comprising:

attaching individual pins to a plurality of contact pads on a surface of a package substrate by solder reflow; and

selectively applying an encapsulation material about solder joints associated with said individual pins, said encapsulation material to maintain a location of said individual pins on said package substrate during subsequent high temperature processing.

33. (New) The method of claim 32, wherein attaching individual pins includes:

placing said individual pins in a jig;

applying solder to at least one of the following: said individual pins and said contact pads;

aligning said jig with said package substrate; and

applying pressure to said jig at a temperature that equals or exceeds a melting temperature of said solder.

34. (New) The method of claim 32, wherein:

applying an encapsulation material includes applying a no flow material.

35. (New) The method of claim 32, wherein:

said encapsulation material includes at least one of the following: an epoxy-based material and a polyimide-based material.

REMARKS

In response to the Office Action dated 18 July 2002, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-13 are pending in the application. Claims 1 and 6-13 are rejected, and claims 2-5 are objected to. Claims 10 and 11 will be amended and new claims 23-35 will be added upon entry of the present amendment. No new matter has been added.

Allowable Subject Matter

The Office Action indicated that claims 2-5 would be allowable if rewritten in independent form. The applicant reserves the right to rewrite claims 2-5 in independent form, but believes that the base claim 1 from which they depend is allowable in view of the remarks made herein.

Rejection of Claims under §103

Claims 1, 7, and 9 were rejected under 35 U.S.C.§103(a) as being unpatentable over Hashimoto (U.S. Patent No. 5,943,217) in view of Capote et al. (U.S. Patent No. 6,297,560, Capote). The applicant respectfully traverses.

Capote issued on 2 October 2001, which is after the 27 September 2001 filing date of the above-identified application. The applicant does not admit that Capote is prior art, and reserves the right to swear behind Capote at a later date.

Claim 1 recites a method for use in assembling a microelectronic circuit package comprising, among other elements, applying a polymer material to a surface of a package

substrate, attaching pins to said package substrate, and allowing said polymer material to cure about solder joints associated with said pins.

Hashimoto relates to a printed circuit board and describes, in column 11, lines 22-35, supplying a flux 19 in which solder layers 11 and outer leads 7 are immersed, and the outer leads 7 and lands 8 are then heated and connected.

Hashimoto is deficient as a reference in that Hashimoto does not show, among other things, a polymer material or the act of allowing said polymer material to cure as are recited in claim 1.

The Office Action stated that "[a]lthough Hashimoto does not explicity teach the step of allowing the flux material 19 to cure, this feature is taken to be inherent for the flux material 19 in Hashimoto's device." Office Action, pages 2-3. The MPEP states the following with regard to rejections based on inherency:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." MPEP 2112 (emphasis in original).

The applicant respectfully submits that the Office Action has not provided a basis in fact and/or technical reasoning to reasonably support the determination that Hashimoto necessarily includes the step of allowing the flux material 19 to cure.

Capote relates to a semiconductor flip-chip assembly and mentions a polymer flux layer 23 in column 7, lines 31-32.

The MPEP states the following with regard to rejections under 35 USC § 103:

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143. Another Federal Circuit opinion states that the suggestion or motivation to combine references must be found in the prior art. MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

The Office Action stated on page 3 that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the well known polymer flux , as taught by Capote et al, to Hashimoto's structure, since it has been held to be within the general skill of a worker..." The Office Action did not cite prior art as the source of this motivation for combining Hashimoto and Capote. The applicant respectfully submits that there is no demonstrated motivation in the prior art for combining Hashimoto and Capote in the manner put forth in the Office Action.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 1 has **not** been established in the Office Action, and that claim 1 is in condition for allowance. Claims 7 and 9 are dependent on claim 1, and recite further limitations with respect to claim 1. For reasons analogous to those stated above, and the features in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 7 and 9 has **not** been established in the Office Action, and that claims 7 and 9 are in condition for allowance.

Claims 6 and 8 were rejected under 35 U.S.C.§103(a) as being unpatentable over Hashimoto in view of Capote and further in view of Variot et al. (U.S. Patent No. 6,088,914, Variot). The applicant respectfully traverses.

Variot relates to planarizing an array of solder balls. Regarding claim 6, Variot mentions in column 5, lines 41-44, screen printing solder paste on to contacts. The Office Action stated on pages 3-4 that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to apply screen-printed process step to the proposed process of Hashimoto and Variot et al to form the polymer flux material on the substrate since such process step is conventionally applied..." With reference to the discussion of 35 USC § 103 above, the Office Action did not cite prior art as the source of this motivation for combining Hashimoto, Capote, and Variot. Furthermore, Variot has not been shown to provide a motivation for combining Hashimoto and Capote that is missing as discussed above. The applicant respectfully submits that there is no demonstrated motivation in the prior art for combining Hashimoto, Capote, and Variot in the manner put forth in the Office Action.

Regarding claim 8, the Office Action has not provided a basis in fact and/or technical reasoning to reasonably support the determination that Variot necessarily includes a no flow material.

Claims 6 and 8 are dependent on claim 1, and recite further limitations with respect to claim 1. For reasons analogous to those stated above, and the features in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 6 and 8 has **not** been established in the Office Action, and that claims 6 and 8 are in condition for allowance.

Claims 10 and 12-13 were rejected under 35 U.S.C.§103(a) as being unpatentable over Bronson et al. (U.S. Patent No. 5,288,944, Bronson). The applicant respectfully traverses.

Amended claim 10 recites a method for use during fabrication of a microelectronic device package comprising, among other elements, attaching individual pins to a plurality of contact pads by solder reflow and selectively applying an encapsulation material about solder joints associated with said individual pins.

Bronson relates to a pinned ceramic chip carrier. Bronson shows in Figure 2 and describes in column 8, lines 11-45 a pinned ceramic chip carrier 110 with pins 170 attached to contact pads 140 with solder 190. Heads 180 of the pins 170, the solder 190, and the contact pads 140 are encapsulated in a region of material 200. The material 200 is shown in Figure 2 as blanketing all of the connections. Bronson does not show selectively applying an encapsulation material about solder joints associated with said individual pins as is recited in claim 10.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 10 has **not** been established in the Office Action, and that claim 10 is in condition for allowance. Claims 12-13 are dependent on claim 10, and recite further limitations with respect to claim 10. For reasons analogous to those stated above, and the features in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 12-13 has **not** been established in the Office Action, and that claims 12-13 are in condition for allowance.

Claim 11 was rejected under 35 U.S.C.§103(a) as being unpatentable over Bronson in view of Iyogi et al. (U.S. Patent No. 4,835,344, Iyogi). The applicant respectfully traverses.

Iyogi relates to a method for manufacturing electronic parts. Iyogi does not show selectively applying an encapsulation material about solder joints associated with said individual pins as is recited in claim 10. Iyogi does not supply the elements missing in Bronson.

Claim 11 is dependent on claim 10, and recites further limitations with respect to claim 10. For reasons analogous to those stated above, and the features in the claim, the applicant respectfully submits that a *prima facie* case of obviousness of claim 11 has **not** been established in the Office Action, and that claim 11 is in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date 18 December 2002 By _____

Robert E. Mates
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 18 day of December, 2002.

Jane Sagers
Name

Signature